Science and Technology – Digital Electronics

1. Digital Electronics and Boolean Algebra. **Brief Introduction to its Origins**, Part 1/2

Digital Electronics, in its **Physical** and **Mathematical** components, forms the basis of the creation of immeasurable Electronic Devices that are currently part of our lives, such as: the Internet, Computers, Tablets, Mobile Phones, Robots, etc. However, in the Mathematical component, it is **Boolean Algebra** which constitutes its **Fundamental Theoretical Tool** and that will allow its development.

The Boolean Algebra genesis lies in Antiquity among Sophists and Philosophers such as **Parmenides**, **Plato** and **Aristotle.** The latter studied, in greater detail, the "Logical Structure of Argumentation", paving the way, in the nineteenth and twentieth centuries, to the development of **Deductive Logics**, among them, **Classical Logic**, also called **Binary Logic** (True-False), **Propositional Calculus** or **First-Order Predicates Calculus**.

The development of **Boolean Algebra**, as we know it today, had contributions of the following works by: **George Boole** himself (1815-1864), "Mathematical Analysis of Logic" and "An Investigation into the Laws of Thought"; **Augustus De Morgan** (1806-1871), "Formal Logic" (**De Morgan Theorem**). (The *Part 2/2 is presented in "Digital Electronics II" Issue*).

2. The Stamps, S273 (6/1) to (6/6)

In the Stamps, S273 (6/1) to (6/6), for **two Input Variables**, the **Truth Tables**, the **Boolean Expressions**, the **Logical Symbols**, the **Basic Electronic Circuits** and the **Venn Diagrams** are presented, for the **NOT**, **AND** and **OR Gates.**

2.1. Truth Table, **Boolean Expression** and **Logical Symbol**, S273 (6/1) to (6/3)

In Digital Electronics, the **Truth Table** is a Mathematical Table composed of **n+1 Columns** and **2^n+1 Rows**.

The first **n Columns**, located on the **Left**, are related to the **n Input Variables (A**, **B**, **C ... N)** and the **Last Column**, located on the **Right**, to the **Output (S)**, as the result of the Logical Operation of the Input Expression.

In the **First Line** are presented the n Input Variables (A, B, C ... N) and in the **Remaining Lines**, all possible **Combinations** or **Hypotheses** related to the n Input Variables (A, B, C ... N) and the corresponding Output (S) values, as the result of the Logical Operation of the Input Expression.

The **Boolean Expression** is the mathematical representation of the **Logical Expression**.

The **Logical Symbol** is a graphical representation of the Gate or Logical Operator.

2.2. Basic Electronic Circuit and **Venn Diagram**, Stamps S273 (6/4) to (6/6)

Taking into consideration that the electronic implementation of the **Logical Gates**, presented in the Stamps, uses **Bipolar Junction Transistors**, **NPN Type** and **Common Emitter Configuration**, it was decided to make its brief introduction below, in order to make its operation easier to understand.

So, it is:

Bipolar: Because it uses either **Electrons** or **Holes** as **Charge Carrier**;

Type N: Because it consists of **2 PN Junctions** connected back-to-back that share a common terminal, **Type P**. (A semiconductor layer, Type P, is inserted between two semiconductor layers, Type N). The **Electrodes** connected to each of these layers are called: **Emitter**, **Base** and **Collector**;

Common Emitter: Because an **Input Signal** is applied between the **Base** and the **Emitter** and an **Output Signal** is obtained between the **Collector** and the **Emitter**.

For a Transistor to function properly, **Direct Polarization Voltages** (**Forward-biased** or **Reverse-biased)** are applied to its **Junctions**.

When the **Voltage** applied to the **Type P Terminal** is higher than that applied to the **Type N Terminal**, with a difference overcoming the **Barrier Voltage**, typically around **0.7V** for the **Silicon Diode**, the **Junction** is **Forward-biased**. On the contrary, when the Voltage applied to a **Type N Terminal** is higher than that applied to the **Type P Terminal**, the Junction is **Reverse-biased**.

According to the **Polarization** applied to the **Emitter** and **Collector Junctions**, the Transistor may work in the:

a) **Active Region (**as an **Amplifier**). See Figure a) below

In this operation mode, the **Base-Collector Junction** is **Reverse-biased** and the **Base-Emitter Junction** is **Forward-biased**.

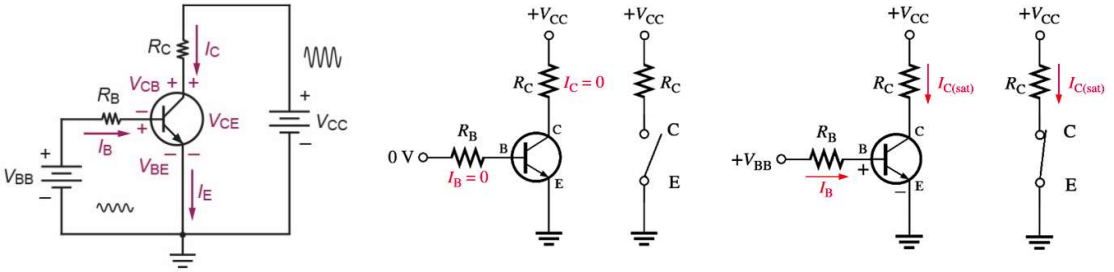
The $\mathbf{I_B}$ Current entering the Base-Emitter circuit controls the $\mathbf{I_C}$ Current in the Collector Circuit. **Minor** changes in the Base-Emitter Current result in **Substantial** changes in the Collector Current, (**Amplification**) $\mathbf{I_C = \beta I_B}$;

b) **Cut-off Region (**as an **Open Switch**). See Figure b) below

Both Junctions are **Reverse-biased**, not circulating Current through them ($\mathbf{I_E = I_B = I_C = 0}$). The Transistor behaves like an **Open Switch** (**OFF**), representing the **Logical Value 0**;

c) **Saturation Region (**as a **Closed Switch)**. See Figure c) below

Both Junctions are **Forward-biased**, circulating Current through the Junctions, $\mathbf{I_C = I_E}$. The Transistor behaves like a **Closed Switch** (**ON**), representing the **Logical Value 1**.



a) Active b) Cut-off c) Saturation

Applying what was previously expressed and taking the **Basic Circuit** of the **Gate OR**, Stamp **S273 (6/6)**, as an example, we can confirm its Truth Table.

Therefore:

When in **both Inputs A** and **B**, the Voltage is "**Low**, **0**", the Junctions of both T1 Transistors are Reverse-biased and they work on the Cutoff Region. There is no Current between the Collector and the Emitter of both Transistors T1 (Open Circuit) and the **Output Voltage** is also "**Low**, **0**", nearly 0 V;

When, in **one** or **both Inputs A** and **B**, the Voltage is "**High**, **1**", the Junctions of one or both T1 Transistors are Forward-biased and this or these work in Saturation Region. Current passes between the Collector and the Emitter of one or both Transistors T1 (Closed Circuit) and the **Output Voltage** is "**High**, **1**", nearly V_{CC} V.

The **Venn Diagram** (John Venn 1834-1923), is a **Graphical Representation** of the relationships between Sets (Group of Things that Share the Same Property), in which the **Universal Set U** is represented by a **Rectangle** and **Specific Sets A**, **B**, **... N**, are represented by **Ovals** or **Circles** that show the existing relationships among each other.

In the case of a **single Set A**, (See Stamp S273 (6/4)), there are elements that belong to A and Elements that do not belong to it. Those that do not belong to the Set correspond in the **Set Theory** to "**Complementarity**, **c**" and in **Digital Electronics** to the **Logical Negation** or **Operator NOT**.

If **Sets A** and **B partially overlap**, (See Stamp S273 (6/5)), there are Common Elements to both and Elements that belong exclusively to one of them. The **Common Elements** in the **Set Theory** corresponds to the "**Intersection**, ∩" and in **Digital Electronics** to the **Logical Multiplication** or **Operator AND**.

The **Set of Elements** belonging, **either** to **Set A** or **Set B** or **both**, (See Stamp S273 (6/6)), in the **Set Theory**, corresponds to the "**Union**, ∪", and in **Digital Electronics** to the **Logical Addition** or **Operator OR**.

3. The Sheetlet, **Postulates**

Postulate, also called **Axiom**, is understood as a **Premise** or **Statement** that is accepted as **True** without the need for **Demonstration**. In the lower margin of the Sheetlet, **5 Postulates** relating to the Operations "+ and • (OR and AND)" are presented.

4. The Souvenir Sheet, **Half-Adder Circuits**, B 229 (1/1)

Presented in the **Souvenir Sheet** are: two Electronic Circuits (I and II) called **Half-Adder (**the **Full-Adder Circuit** will be presented in the next Issue, called "Digital Electronics II") which allow the **Addition** of **Two Bits**, being **S** its **Sum** and **Ts** the **Carry Out**; the Truth Table of the Operation; the Logical Expression of the Sum and also an Image of George Boole.

The **Logical Expression of the Circuit** is obtained directly from the Truth Table, corresponding **S** = **(0110)** to $\bar{A}B+A\bar{B}$ or to **A⊕B** (**XOR**, **EXCLUSIVE OR**, to be presented in the next Issue, called "Digital Electronics II") and **Ts = (0001)** to **A•B**.

5. The First Day Covers (FDC), **Karnaugh Map**, ENA274 and ENB 231

Through the **Simplification** obtained by the use of the **Karnaugh Map**, the **11 Initial Terms** of Expression F were reduced only to **3 Final Terms**, not containing these the totality of **Variables**, which constitutes a considerable **saving** of **Electronic Circuits**.

To achieve this, **3 Rectangles**, **Green**, **Red** and **Blue** were formed in order to include all existing **1's** of the **16** Map **Cells** which will allow to obtain, respectively, the 3 Simplified Final Terms, $\mathbf{A\overline{C}}$, **D** and $\mathbf{\overline{A}BC}$.

Taking the **Green Rectangle** as an example, the Term $\mathbf{A\overline{C}}$ was obtained as follows.
As the Variable:

"A" in (AB, 11, 10), always takes the value **1**, remains as **A**;
"B" in (AB, 11, 10), takes the different values **1** and **0**, is eliminated;
"C" in (CD, 00, 01), always takes the value **0**, remains as $\mathbf{\overline{C}}$;
"D" in (CD, 00, 01), takes different values **0** and **1**, is eliminated.

Applying the same principles to the **Red** and **Blue Rectangles**, we obtain, respectively, the terms **D** and $\mathbf{\overline{A}BC}$.

Author of the text and concept of the issue: Carlos Alberto Roldão Lopes